Xinhua Lai

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Education

University of Chinese Academy of Sciences (UCAS) 2021 – Present

Ph.D. Candidate in Computer Applied Technology
(Research Interests: AI for EDA, Chip Placement/Routing; Advisor: Prof. Jungang Xu)

Central South University (CSU) 2016 – 2019

Master of Engineering in Software Engineering
(Research Interests: Deep Learning Applications; Advisor: Prof. Xuegong Chen)

Jingdezhen Ceramic University (JCU) 2010 – 2014

Bachelor of Engineering in Electronic Science and Technology

Research & Patents

Research Interests

AI for EDA, Chip Placement & Routing, Deep Learning Applications

Accepted Papers

- **Xinhua Lai**, He Liu, Weiguo Li, Yihang Qiu, Miao Liu, Simin Tao, Xingquan Li, Jungang Xu. iPCL-M1: Pre-training of Chip Layout for Metrics Evaluation and Optimization. DAC, 2026. (CCF-A, **Oral Presentation**)
- **Xinhua Lai**, Miao Liu, Xingquan Li, Yihang Qiu, Shijian Chen, Xinhao Li, and Jungang Xu. "iPO: Constant Liar Parameter Optimization for Placement with Representation and Transfer Learning." ACM TODAES, 2025. (Trans / CCF-B)
- Miao Liu, **Xinhua Lai**, Liwei Ni, Xingyu Meng, Rui Wang, Junfeng Liu, Xingquan Li, Jungang Xu. CircuitFlow: Learning Dynamic Representations for Logic Optimization. TCAD, 2026. (CCF-A)
- Xingquan Li, Weiguo Li, **Xinhua Lai**. iPCL: Pre-training for Chip Layout (Invited). ASPDAC, 2026. (CCF-C)
- Yihang Qiu, Zengrong Huang, Simin Tao, Hongda Zhang, Weiguo Li, **Xinhua Lai**, Rui Wang, Weiqiang Wang, Xingquan Li, "AiEDA: An Open-Source AI-Aided Design Library." TCAD, 2025. (CCF-A)
- Miao Liu, Liwei Ni, Junfeng Liu, Xingyu Meng, Rui Wang, Xiaoze Lin, **Xinhua Lai**, Xingquan Li, and Jungang Xu. TODAES, 2025. (CCF-B)
- Yihang Qiu, Zengrong Huang, Weiguo Li, **Xinhua Lai**, Rui Wang, He Liu, Ping Zhou, Simin Tao, Junfeng Liu, Yifang Li, Xingquan Li, "AiEDA-2.0: An Open-source AI-Aided Design Library." ISEDA, 2025. (EI)

Papers Under Review

- **Xinhua Lai**, et al., GT-Fusion: LLM Semantic and Spatio-Topological Integration for PPA Prediction and Optimization. ISEDA. 2026. (1st Author)
- **Xinhua Lai**, et al., "AiMPlacer: A Parallelized Macro Placer with Reinforcement Learning and Transformers." Neurocomputing, 2026. (SCI Q2 / Co-1st Author)

Patents

- Jungang Xu (Advisor), **Xinhua Lai**. Training Method and Apparatus for Chip Design Metric Generation Model, CN202510301467.8
- Jungang Xu (Advisor), **Xinhua Lai**. Chip Placement Method and Apparatus, CN202411422151.6

- Jungang Xu (Advisor), **Xinhua Lai**. Chip Placement Information Generation Method and Apparatus, CN202411421642.9
- Ling Wang, **Xinhua Lai**. Resume Parsing Method and Apparatus, CN202210361622.1 (2nd Author)

Work & Internship Experience

Peng Cheng Laboratory 2024.05 – Present

Algorithm & Model Researcher Participated in the "AI for EDA" research initiative. Responsible for algorithm and model design, exploring the design space in the physical design stage, and applying Large Language Models (LLMs) to physical design processes.

Lijiang Culture and Tourism College (School of AI) 2025.05 – 2025.06

Adjunct Lecturer

- Taught the experimental course *Comprehensive AI Training*, independently designing course experiments and assignments, receiving excellent feedback from students.
- Mentored undergraduate students from proposal to thesis writing, guiding them to successfully complete their graduation designs.

University of Chinese Academy of Sciences (UCAS) 2021.09 – 2025.12

Teaching Assistant **in** *UCAS*

- Served as the primary TA for the doctoral course *Advanced Data Management*, providing online/offline tutoring, assisting in experiment design, and developing code implementations and manuals.
- Acted as TA for *Python Programming*, *C++ Programming*, and *Advanced Software Engineering*, responsible for grading assignments and final exams.

CCIP Laboratory, UCAS 2020.08 – 2021.08

Research Assistant Joined the lab in advance under the advisor's arrangement, participating in project development and algorithm implementation to support scientific research tasks.

Huawei Technologies Co., Ltd. 2019.06 – 2020.07

C++ R&D Engineer Responsible for the algorithm development and optimization of the WDM End-to-End (E2E) module in the NCE (formerly u2000) Network Management System. Utilized C++ to optimize path search and calculation algorithms, enhancing network element signal transmission efficiency, and supported real-time service monitoring and restoration.

Project Experience

Multimodal LLM-based Framework for Chip PPA Prediction & Optimization (ISEDA 2026)
2025.11 – Present

- Proposed a tri-modal PPA prediction framework integrating LLMs, GNNs, and UNet to bridge the "modality gap" between the logical netlist design intent and physical layout geometric features.
- Designed a cross-modal injection mechanism that utilizes LLMs to extract textual design semantics, aligns them with global topological features from GNNs, and injects them into UNet's spatial features, achieving unified modeling of semantic, topological, and geometric views.
- Validated on the Skywater 130nm benchmark: Reduced visual congestion prediction error (MAE) by 28.3% and path delay prediction error (RMSE) by 37.5% compared to single-modal (Pure UNet) and bi-modal baselines, proving the necessity of multimodal fusion.
- Integrated the prediction model into an open-source EDA tool (iEDA) to build a closed-loop optimization flow, guiding the placer to dynamically adjust strategies based on prediction feedback. Reduced maximum overflow by 16.1% in congestion-constrained designs and improved WNS by 3.3% in timing-constrained designs.

Pre-trained Model Framework for Chip Routing Generation & Evaluation (DAC 2026)
2024.11 – Present

- Proposed a pre-training framework for chip layout based on a symbolic space, establishing a "Generate-Evaluate-Optimize-Generate" (GEOG) closed-loop paradigm to solve the fragmentation of evaluation and optimization in traditional physical design.
- Constructed a universal layout symbolic system and pre-trained a generative model using commercial-grade routing data. Achieved high-precision generation from pin coordinates to 3D routing paths, with Mean Relative Error (MRE) of endpoints <1% and absolute error <1 routing track.
- Developed a lightweight metric evaluation model to rapidly predict timing, power, and parasitic parameters directly from routing patterns without invoking the full STA flow, achieving a 336x inference speedup compared to traditional tools (iSTA).
- Designed a path optimization strategy based on real-time evaluation feedback, significantly enhancing routing quality. Experiments showed improvements in wirelength, delay, and slew by 10.49%, 13.03%, and 14.85% respectively, outperforming commercial tools (Innovus) in key metrics.

Core Module Development for AiEDA Open-Source Platform 2024.10 – 2025.03

- **Algorithm Engineering & Deployment**: Integrated the self-developed cross-design parameter optimization algorithm (iPO) into the AiEDA infrastructure, building an automated tuning flow supporting parallel search and transfer learning for adaptive configuration of key physical design parameters.
- **Architecture Design & Decoupling**: Employed the **Bridge pattern** to decouple optimization algorithms (e.g., Bayesian Optimization, Evolutionary Algorithms) from underlying EDA tools (e.g., iEDA, DREAMPlace), and utilized the **Facade pattern** to encapsulate complex parameter extraction/configuration interfaces, drastically reducing module coupling.
- **Platform Efficiency Enhancement**: Standardized interface designs to significantly improve platform scalability, supporting the rapid integration of new tools. The optimized architecture effectively supported cross-design parameter reuse, accelerating toolchain deployment and iteration across varied design scenarios.

AiMPlacer: Parallel Macro Placer with Reinforcement Learning and Transformers (Neurocomputing 2026) 2024.05 – 2024.12

- Proposed AiMPlacer, a Reinforcement Learning (RL)-based macro placement framework that frames the problem as a visual representation learning task, resolving bottlenecks of improper feature embedding and slow convergence in existing RL methods.
- Designed a Transformer-based visual encoder integrated with side-band information embedding to deeply fuse global visual features of the layout with netlist topologies (node/edge attributes), significantly enhancing layout feature representation.
- Developed a Parallel Advantage Actor-Critic (PA2C) algorithm introducing hybrid asynchronous/synchronous gradient updates for multi-process parallel exploration. Achieved a 2.7x training speedup (reducing training time from 16 to 6 hours) using 4 parallel processes.
- Validated on ISPD2005 and TILOS benchmarks: Improved HPWL by 6.8% compared to DREAMPlace and 9.7% compared to DeepPlace. Training convergence speed increased by over 3x compared to traditional A2C and PPO algorithms.

iPO: Automated Placement Parameter Configuration Framework via Transfer Learning (TODAES 2025) 2023.11 – 2025.05

- Proposed iPO, a cross-design placement parameter optimization framework combining representation learning and transfer learning, addressing the pain points of manual tuning reliance and poor cross-design reusability in traditional tools (DREAMPlace, iEDA).
- Designed a circuit representation module based on Graph2vec and Weisfeiler-Lehman kernels to encode netlist topologies into high-dimensional vectors. Implemented a parameter transfer strategy based on cosine similarity clustering, effectively utilizing historical data to guide new design optimizations.
- Introduced the "Constant Liar" heuristic strategy to support asynchronous parallel search, overcoming the sequential execution bottleneck in Bayesian Optimization. Achieved an 18x speedup in parameter search

using 10 parallel processes.

- On the ISPD2015 benchmark, improved HPWL by 11% and reduced congestion by 12.3% compared to AutoDMP, with search iterations accelerated by 3.49x. On iEDA 28nm designs, further optimized TNS by 2.8% compared to manual tuning.

Technical Skills

- **Programming Languages**: Python, C++, Java; Familiar with Design Patterns (e.g., Singleton, Factory, Observer, Bridge, Facade).
- **Deep Learning**: PyTorch (Research modeling, training, and deployment); Systematic knowledge of Machine Learning and Deep Learning.
- **Development Environment**: Linux, Vim/Neovim, CMake; Proficient in debugging and version control (Git).

Awards & Honors

Rising Star Award, openDACS 2025 Open-Source EDA & Chip	2025
Excellence Award, openDACS 2025 Open-Source EDA & Chip Competition	2025
Best Poster, "AI for Science" Graduate Academic Forum, UCAS	2025
3rd Place, Xiakedao EDA^2 Mixed-Size Placement Algorithm Competition	2025.07
Academic Scholarship for Graduate Students, UCAS (Awarded 3 times)	2021-2023
Merit Student, UCAS	2021

Miscellaneous

- English: CET-6 (Fluent)
- GitHub: 1.2k+ ⋆ in SivanLaai
- Personal Blog: in https://blog.laais.cn

Professional Summary

Dedicated to AI for EDA research. First author of top-tier papers including DAC 2026 (Oral) and ACM TODAES, possessing comprehensive algorithm engineering capabilities (Huawei C++ R&D, AiEDA open-source core contributor). Proficient in full-stack development from scientific research innovation to model deployment, with deep practical experience in pre-trained large models, multimodal fusion, and generative frameworks. Passionate about open-source communities and knowledge sharing (1.2k+ stars on GitHub), thriving on driving advanced technology implementation through team collaboration.